APPARATUS, METHODS AND ARTICLES OF MANUFACTURE FOR DYNAMIC DIFFERENTIAL DELAY CORRECTION

FIELD OF THE INVENTION

[0001] The invention relates to the transfer of electromagnetic waves. More particularly, the invention relates to a system for processing electromagnetic signals, and more particularly to adjusting for signal propagation delays in systems processing electromagnetic waves.

BACKGROUND OF THE INVENTION

[0002] Electromagnetic waves may be transferred from place to place through a conductor. In wired transmission, the conductor is usually a wire or other solid substance. In wireless transmission, the conductor is usually an ambient substance, such as air, water, etc. In wireless connections a transmitter is usually used to transfer a wave and a receiver to receive a wave. A transceiver combines the functions of both transmitter and receiver in one system. A transmitter typically converts electrical energy into a signal, which is then broadcast via an antenna to a receiver's antenna. Repeaters, middle stations, etc. may be used as intermediates in the transmission to sustain the integrity of the transmitted wave.

[0003] The electrical energy input into a transmitter usually is modulated into a basic transmission or carrier signal by overlaying some intelligence upon the energy – speech, data, etc. – in the form of an information signal, and the receiver typically demodulates the modulated carrier signal, once received, into a copy of the initial intelligence sent by the transmitter.

[0004] In order to accomplish their function, transmitters, receivers, and tranceivers are comprised of various building block components. The information signal, for example, may be generated or modulated by one or more transducers, such as a microphone. It may also be

generated by a modulator, such as an analog modem. The modulation of the information signal onto the carrier signal may be done by a mixer and the energy or carrier wave itself is usually generated by an oscillator. An amplifier is usually used at one or more places in the transmitter circuitry to boost the signal strength, to provide power to active components, etc. Similarly, one or more filters are usually used as well, to clean up the input signal, the outputted signal, etc. An antenna is used to broadcast the signal, and a power supply will supply power as needed.

[0005] All of these system components may introduce delay into the propagation of a signal through the system, which may cause distortion in the signal outputted from the processing system. In some systems, aspects of the electromagnetic wave, such as amplitude and phase information, may be processed along different paths and with difference components. Some of these components may be analog in nature and some digital. Because of this, there may be a difference in delay, or differential delay, between each aspect of the electromagnetic wave when they are recombined, which may cause unwanted distortion in the processed output signal.

[0006] Because of drawbacks in conventional systems, it would be desirable to provide more efficient and precise methods and articles of manufacture processing electromagnetic waves in this manner.

SUMMARY OF THE INVENTION

[0007] The invention comprises systems, methods and articles of manufacture for transmitting and receiving electromagnetic waves and signals. Embodiments of the invention may incorporate a system for dynamically correcting an electromagnetic wave by processing two or more aspects of the electromagnetic wave along two or more separate signal paths; comparing an expected value for at least one of the aspects of the electromagnetic wave with an actual value

for the aspect of the electromagnetic wave to generate a correction signal; and applying the correction signal to another aspect of the electromagnetic wave.

[0008] In one embodiment, the aspects of the electromagnetic wave to be processed may be amplitude and phase, where the comparison may be along the phase path and the adjustment along an analog portion of the amplitude path. A digital phase locked loop may be used for the comparison and to generate the correction signal; and a bank of pipeline registers may be used to adjust the amplitude path.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] For the purpose of illustrating the invention, there is shown in the drawings at least one embodiment, which is presently preferred; it being understood, however, that this invention is not limited to the precise arrangements, methods and instrumentalities shown.

[0010] Figure 1 shows an embodiment of a system for processing an electromagnetic wave.

[0011] Figure 2 shows an embodiment of a signal correction circuit.

[0012] Figure 3 shows an embodiment of a wave transmitter.

DETAILED DESCRIPTION OF THE INVENTION

[0013] Embodiments of the invention include apparatus, methods and articles of manufacture for providing signal correction in the processing electromagnetic waves, such as for transmitting and receiving information signals. It should be noted that the word "signal" is used herein to describe an electromagnetic wave that has been modulated in some fashion, usually by the impression of intelligence upon the wave, for example imposing data upon a carrier wave. It should also be noted that the use of "signal" and "wave" in the singular includes the plural (or

multiple signals and waves respectively) as often systems for processing electromagnetic waves, such as transmitters, receivers and transceivers, generate more than one signal and/or wave in the normal course of their operation. For example, multiple harmonics of a baseband signal might be desirably generated as in amplitude modulation; multiple frequencies might be generated, etc.

[0014] Embodiments of the invention may be entirely comprised of hardware, software and/or may be a combination of software and hardware. Accordingly, individual blocks and combinations of blocks in the drawings support combinations of means for performing the specified functions and/or combinations of steps for performing the specified functions. Each of the blocks of the drawings, and combinations of blocks of the drawings, may be embodied in many different ways, as is well known to those of skill in the art.

[0015] Figure 1 illustrates a generalization of a circuit in which a differential delay may occur between aspects of an electromagnetic wave being processed by a system. As shown in Figure 1, processing system 100 may include a source of an electromagnetic signal 102, which may provide information regarding aspects of the wave, such as amplitude and phase, out along different signal paths. Each signal path may comprise one or more analog components (110, 112, and 122) and digital signal processing components (104, 106, 108, 118, and 120). Each of the digital processing components may be timed from the same common clock source 116.

[0016] For purposes of the embodiment disclosed herein, it will be assumed that the amplitude and phase signals start out time aligned from source 102. However, those of ordinary skill in the art will appreciate that the invention is not limited thereto. Because the amplitude and phase paths require different processing in differing components, the timing of the signals may diverge as the signals traverse the various processing blocks. Thus, when the signals are recombined at recombining circuit 114 the signal may suffer from significant distortion.

[0017] For purposes of illustration the phase path is shown as the dominant delay. However, those of ordinary skill in the art will appreciate that the converse is possible as well. If the phase is considered to be the dominant delay, then delay must be added to the amplitude path to equalize the paths. A digital delay adjust component 124 and an analog delay adjust component 126 may be added to perform this delay equalization.

[0018] In order for processing system 100 to perform acceptably, the delays should be controlled in accordance with the equation: Phase_delay_total = Amp_delay_total + Digital_Delay_Adjust + Analog_Delay_Adjust. As long as the difference between the left and right sides of this expression is within an acceptable tolerance for the particular processing operation, then the performance of the system will be deemed to be acceptable.

[0019] It is also assumed that the delay caused by the digital blocks is determined primarily by clock 116 and is invariant over temperature, processing and voltage to within the tolerance of clock 116, and so may be pre-determined. Also, any clock variability may be assumed to be applicable to both paths and may be normalized out.

[0020] Thus, the difference in the amplitude and phase paths due to digital clocking may be easily computed by taking the difference in the number of clock periods each signal takes through each path and then adding this difference to the amplitude path (in this example) using digital delay adjust component 124. The mechanism used for digital delay adjust 124 is not particularly limited, and may comprise, for example, one or more pipeline registers. Digital delay adjust 124 may be hardwired to a fixed delay at the time of design or may be programmable for active adjustment of the delay compensation.

[0021] As a result, the major cause of variations in delay over temperature, process, and voltage may be attributable primarily to any analog components in the paths. Variations in the

analog component paths may also be detected and compensated for using analog delay adjust 126. Detection of the differential delay may be performed by quantizing the phase signal just prior to the recombining in recombining circuit 126 and then comparing this quantized signal to the desired or expected phase response. In the illustrated embodiment, this may be accomplished using quantizer 128 and digital phase-locked loop (DPLL) 130.

[0022] DPLL 130 may be used to perform an alignment of the expected phase and the actual phase signals. DPLL 130 may receive the expected phase signal from an earlier digital processing component, in this example block 106. Quantizer 128 may receive the actual phase signal outputted from analog component 112 and produces a quantized signal representing the actual phase signal for inputting to DPLL 130. DPLL 130 receives this quantized, or sampled actual phase signal from quantizer 128 and produces a delay adjust control signal. The delay adjust control signal may be based upon the magnitude of the delay variation.

[0023] The manner in which this may be accomplished is not particularly limited. One embodiment is shown in Figure 2. As shown in Figure 2, the expected differentiated phase signal may be used to drive a phase accumulator 164 in a conventional manner to produce a reference signal representative of the expected phase for the processed output signal. Those of ordinary skill in the art will appreciate that the number of bits used in phase accumulator 164 is not particularly limited. In the illustrated embodiment, the resolution of phase accumulator 164 (i.e, the number of bits) may be equal to that of quantizer 128.

[0024] Quantizer 128, in turn, may be used to sample the actual phase signal. This function may be accomplished in any number of ways, such as by using an A/D converter, which would output a digital signal from quantizer 128 that contains the phase information of the modulated signal. Quantizer 128 may also use a timing signal from clock 116 in a conventional manner.

The timing signal from clock 116 may also be incorporated into the digital signal outputted from quantizer 128.

[0025] This digital output from quantizer 128 may then be inputted to DPLL 130 for comparison with the expected phase signal. For example, this digital signal may be subtracted from the "ideal" reference phase signal at subtractor 154. Subtractor 154 may digitally subtract these two signals to produce an output that is a phase delay error signal, representative of the difference, or delay error, between the expected phase (which is substantially synchronized with the amplitude signal via clock 116) and the actual phase sampled by quantizer 128.

[0026] The delay error signal may then be received by phase detector 144, which may be operated to provide for a direct comparison of the digitally summed expected phase and the actual phase to produce a correction signal representing the amount of correction needed by analog delay adjust component 126.

[0027] The output of phase detector 144 may be passed to decimator 156, which may be used to reduce the sample rate of the loop filter in the DPLL. Decimator 156 may comprise, for example, a cascaded integrator-comb filter (CIC) type, but is not limited thereto. Decimator 156 then feeds loop filter 158, which may comprise, for example an FIR filter having a predetermined response calculated for use with the signal being processed. The feedback output signal of loop filter 158 may then be combined with the expected phase signal at subtractor 160.

[0028] The delay control signal outputted from DPLL 130 may be received by analog delay adjust block 126, which adds or subtracts the appropriate delay to the amplitude path. Analog delay adjust block 126 is not particularly limited and may comprise any mechanism for adjusting the phase is the signal path, such as a bank of pipeline registers clocked at rate that is set high

enough to provide the granularity to bring the amplitude and phase paths into alignment within the tolerance required by processing system 100.

[0029] One embodiment of a system for processing an electromagnetic wave incorporating the invention is illustrated in Figure 3. In this embodiment, a wave transmitter 300 includes a baseband signal source 301 for receiving an input signal that contains intelligence (e.g., voice, data, etc.), an amplitude/phase signal processor 302, wide-band phase modulator 321, differential delay correction circuit 340, delay adjuster 342, power amplifier 305.

[0030] A phase modulated carrier wave from wideband phase modulator 321 is passed to differential delay correction circuit 340. A particular embodiment of differential delay correction circuit 340 may be as shown in Figure 2, as previously described. Differential delay correction circuit 340 quantizes the actual phase signal using quantizer 128 for comparison with the expected phase as received from amplitude/phase signal processor 302. This may be accomplished using DPLL 130, as previously described. DPLL 130 generates a correction signal based upon this comparison. This correction signal may then be passed to delay adjuster 342. As discussed above, delay adjuster 342 is not particularly limited, but may comprise a bank of pipeline registers, for example. Delay adjuster 342 adjusts the delay of amplitude component to reduce or eliminate its differential delay with phase component. In some modulation schemes, such as CDMA for example, it is preferably that the delay tolerance be less than about 10ns.

[0031] While the invention has been described herein in regard to a transmitter, those of ordinary skill in the art will appreciate that the invention is not limited thereto and that other processing systems may be used as well. In some embodiments, a transmitter, receiver, and/or transceiver processing system of the invention may be specialized for particular input signals, carrier waves and output signals, e.g. various types of cell phones, such as CDMA, CDMA2000,

W-CDMA, GSM, TDMA, as well as various other types of devices, both wired and wireless, e.g. Bluetooth, 802.11a, -b, -g, GPS, radar, 1xRTT, radios, GPRS, computers and computer communication devices, handheld devices, etc. Among the modulation schemes supported by the invention are: GMSK, which is used in GSM; GFSK, which is used in DECT & Bluetooth; 8-PSK, which is used in EDGE, OQPSK & HPSK, which are used in IS-2000; p/4 DQPSK, which is used in TDMA; and OFDM, which is used in 802.11.

[0032] The preferred embodiments utilize both analog and digital components insofar as these embodiments manipulate waves and signals requiring both. For example, cell phone embodiments may utilize both analog and digital components. Various types of system architectures may be utilized for constructing the embodiments. Generally an ASIC composition is used in realizing the various architectures. CMOS and/or BiCMOS fabrication techniques may be used as well as a combination of both, e.g. a BiCMOS Phase modulator area combined with a CMOS baseband area. Generally, in the preferred embodiments, transistor speed is a concern, and BiCMOS provides faster speed. Additionally, BiCMOS provides less current drain than an all CMOS configuration.

[0033] The invention improves over the systems of the prior art. The ability to detect amplitude and phase delay mismatch and to adjustment of the delay to align the amplitude and phase paths occurs automatically while in operation substantially reduces expensive calibration time in the factory. This significant benefit is more pronounced since this scheme substantially eliminates the necessity of an embedded host controller, e.g., in a wireless handset, from having to perform a complex algorithm to align the two paths. In conventional systems, this algorithm would have to periodically recalibrate during a wireless phone call to account for significant temperature and voltage variations that can occur within a relatively short periods.

[0034] The transmitter of the invention does not include I/Q modulators, but instead preferably uses a polar modulation system. Conventionally, I/Q modulators have been used with linear modulation schemes. Not using such modulators eliminates the problem of I/Q imbalance that occurs when these modulators are used.

[0035] Having thus described a few particular embodiments of the invention, various alterations, modifications, and improvements will readily occur to those skilled in the art. Such alterations, modifications and improvements as are made obvious by this disclosure are intended to be part of this description though not expressly stated herein, and are intended to be within the spirit and scope of the invention. Accordingly, the foregoing description is by way of example only, and not limiting. The invention is limited only as defined in the following claims and equivalents thereto.